

FEATURES

- RF frequency range of 2300 MHz to 2900 MHz
- IF frequency range of 30 MHz to 450 MHz
- Power conversion gain: 8.5 dB
- SSB noise figure of 9.9 dB
- SSB noise figure with 5 dBm blocker of 21 dB
- Input IP3 of 25 dBm
- Input P1dB of 10.6 dBm
- Typical LO drive of 0 dBm
- Single-ended, 50 Ω RF and LO input ports
- High isolation SPDT LO input switch
- Single-supply operation: 3.3 V to 5 V
- Exposed paddle 5 mm × 5 mm, 20-lead LFCSP
- 1500 V HBM/500 V FICDM ESD performance

APPLICATIONS

- Cellular base station receivers
- Transmit observation receivers
- Radio link downconverters

GENERAL DESCRIPTION

The ADL5353 uses a highly linear, doubly balanced passive mixer core along with integrated RF and LO balancing circuitry to allow for single-ended operation. The ADL5353 incorporates an RF balun, allowing for optimal performance over a 2300 MHz to 2900 MHz. The balanced passive mixer arrangement provides good LO-to-RF leakage, typically better than -39 dBm, and excellent intermodulation performance. The balanced mixer core also provides extremely high input linearity, allowing the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in the degradation of dynamic performance. A high linearity IF buffer amplifier follows the passive mixer core to yield a typical power conversion gain of 8.4 dB and can be used with a wide range of output impedances.

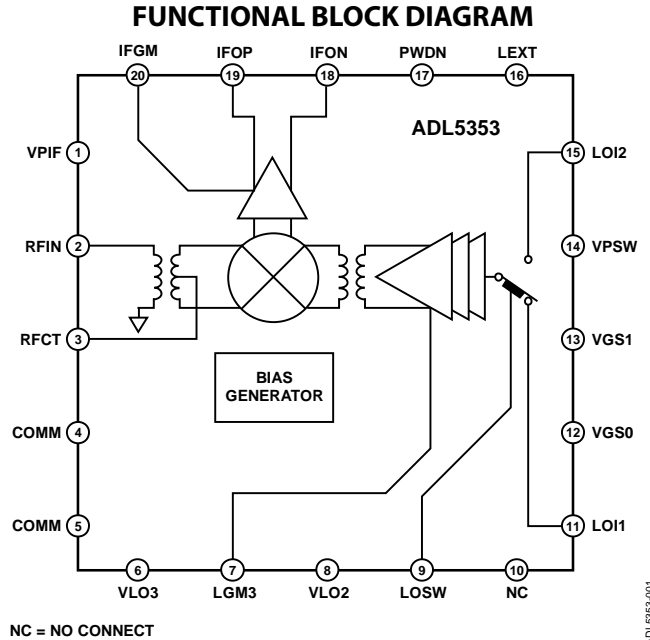


Figure 1.

The ADL5353 provides two switched LO paths that can be used in TDD applications where it is desirable to rapidly switch between two local oscillators. LO current can be externally set using a resistor to minimize dc current commensurate with the desired level of performance. For low voltage applications, the ADL5353 is capable of operation at voltages down to 3.3 V with substantially reduced current. Under low voltage operation, an additional logic pin is provided to power down (<200 μA) the circuit when desired.

The ADL5353 is fabricated using a BiCMOS high performance IC process. The device is available in a 5 mm × 5 mm, 20-lead LFCSP and operates over a -40°C to +85°C temperature range. An evaluation board is also available.

Table 1. Passive Mixers

RF Frequency (MHz)	Single Mixer	Single Mixer and IF Amp	Dual Mixer and IF Amp
500 to 1700	ADL5367	ADL5357	ADL5358
1200 to 2500	ADL5365	ADL5355	ADL5356
2300 to 2900		ADL5353	ADL5854

PrA

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TABLE OF CONTENTS

Features	1	RF Subsystem	8
Applications	1	LO Subsystem	8
General Description	1	Applications Information	10
Functional Block Diagram	1	Basic Connections	10
Specifications	3	IF Port	10
5 V Performance	4	Bias Resistor Selection	10
Absolute Maximum Ratings	5	Mixer VGS Control DAC	10
ESD Caution	5	Evaluation Board	12
Pin Configuration and Function Descriptions	6	Outline Dimensions	15
Typical Performance Characteristics	7	Ordering Guide	15
5 V Performance	7		
Circuit Description	8		

SPECIFICATIONS

$V_S = 5\text{ V}$, $I_S = 190\text{ mA}$, $T_A = 25^\circ\text{C}$, $f_{RF} = 2600\text{ MHz}$, $f_{LO} = 2803\text{ MHz}$, LO power = 0 dBm, $Z_O = 50\ \Omega$, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		TBD		dB
Input Impedance			50		Ω
RF Frequency Range		2300		2900	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, $f = 200\text{ MHz}$		230 0.75		Ω pF
IF Frequency Range		30		450	MHz
DC Bias Voltage ¹	Externally generated	3.3	5.0	5.5	V
LO INTERFACE					
LO Power		-6	0	+10	dBm
Return Loss			TBD		dB
Input Impedance			50		Ω
LO Frequency Range		TBD		TBD	MHz
POWER-DOWN (PWDN) INTERFACE ²					
PWDN Threshold			1.0		V
Logic 0 Level				0.4	V
Logic 1 Level		1.4			V
PWDN Response Time	Device enabled, IF output to 90% of its final level		160		ns
	Device disabled, supply current < 5 mA		220		ns
PWDN Input Bias Current	Device enabled		0.0		μA
	Device disabled		70		μA

¹ Apply the supply voltage from the external circuit through the choke inductors.

² PWDN function is intended for use with $V_S \leq 3.6\text{ V}$ only.

5 V PERFORMANCE

$V_S = 5\text{ V}$, $I_S = 190\text{ mA}$, $T_A = 25^\circ\text{C}$, $f_{RF} = 2600\text{ MHz}$, $f_{LO} = 2803\text{ MHz}$, LO power = 0 dBm, $V_{GS0} = V_{GS1} = 0\text{ V}$, and $Z_O = 50\ \Omega$, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		8.5		dB
Voltage Conversion Gain	$Z_{SOURCE} = 50\ \Omega$, differential $Z_{LOAD} = 200\ \Omega$ differential		14.5		dB
SSB Noise Figure			9.9		dB
SSB Noise Figure Under Blocking	5 dBm blocker present $\pm 10\text{ MHz}$ from wanted RF input, LO source filtered		TBD		dB
Input Third-Order Intercept (IIP3)	$f_{RF1} = 2599.5\text{ MHz}$, $f_{RF2} = 2600.5\text{ MHz}$, $f_{LO} = 2803\text{ MHz}$, each RF tone at -10 dBm		25		dBm
Input Second-Order Intercept (IIP2)	$f_{RF1} = 2600\text{ MHz}$, $f_{RF2} = 2650\text{ MHz}$, $f_{LO} = 2803\text{ MHz}$, each RF tone at -10 dBm		48		dBm
Input 1 dB Compression Point (IP1dB)			10.6		dBm
LO-to-IF Leakage	Unfiltered IF output		-15		dBm
LO-to-RF Leakage			-36		dBm
RF-to-IF Isolation			-28		dBc
IF/2 Spurious	-10 dBm input power		-63		dBc
IF/3 Spurious	-10 dBm input power		-73		dBc
POWER SUPPLY					
Positive Supply Voltage		4.5	5	5.5	V
Quiescent Current	LO supply, resistor programmable		TBD		mA
	IF supply, resistor programmable		TBD		mA
Total Quiescent Current	$V_S = 5\text{ V}$		186		mA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage, V_s	5.5 V
RF Input Level	20 dBm
LO Input Level	13 dBm
IFOP, IFON Bias Voltage	6.0 V
VGS0, VGS1, LOSW, PWDN	5.5 V
Internal Power Dissipation	1.2 W
θ_{JA}	25°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec)	260°C

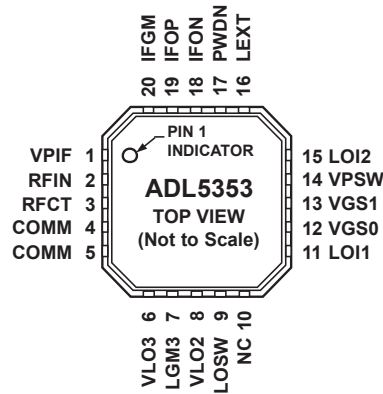
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. NC = NO CONNECT.
 2. EXPOSED PAD. MUST BE SOLDERED TO GROUND.

ADL5353-002

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPIF	Positive Supply Voltage for IF Amplifier.
2	RFIN	RF Input. Must be ac-coupled.
3	RFCT	RF Balun Center Tap (AC Ground).
4, 5	COMM	Device Common (DC Ground).
6, 8	VLO3, VLO2	Positive Supply Voltages for LO Amplifier.
7	LGM3	LO Amplifier Bias Control.
9	LOSW	LO Switch. LOI1 selected for 0 V, and LOI2 selected for 3 V.
10	NC	No Connect.
11, 15	LOI1, LOI2	LO Inputs. Must be ac-coupled.
12, 13	VGS0, VGS1	Mixer Gate Bias Controls. 3 V logic. Ground these pins for nominal setting.
14	VPSW	Positive Supply Voltage for LO Switch.
16	LEXT	IF Return. This pin must be grounded.
17	PWDN	Power Down. Connect this pin to ground for normal operation and connect this pin to 3.0 V for disable mode.
18, 19	IFON, IFOP	Differential IF Outputs (Open Collectors). Each requires an external dc bias.
20	IFGM	IF Amplifier Bias Control.
	EPAD (EP)	Exposed pad. Must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

5 V PERFORMANCE

$V_S = 5\text{ V}$, $I_S = 190\text{ mA}$, $T_A = 25^\circ\text{C}$, $f_{RF} = 2600\text{ MHz}$, $f_{LO} = 2803\text{ MHz}$, LO power = 0 dBm, $R_9 = 1.1\text{ k}\Omega$, $R_{14} = 910\ \Omega$, $V_{GS0} = V_{GS1} = 0\text{ V}$, and $Z_O = 50\ \Omega$, unless otherwise noted.

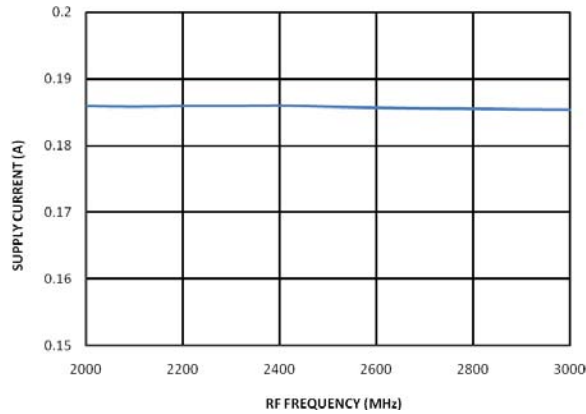


Figure 3. Supply Current vs. RF Frequency

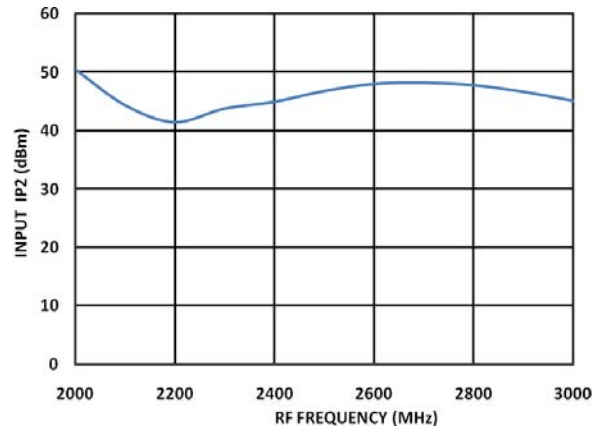


Figure 6. Input IP2 vs. RF Frequency

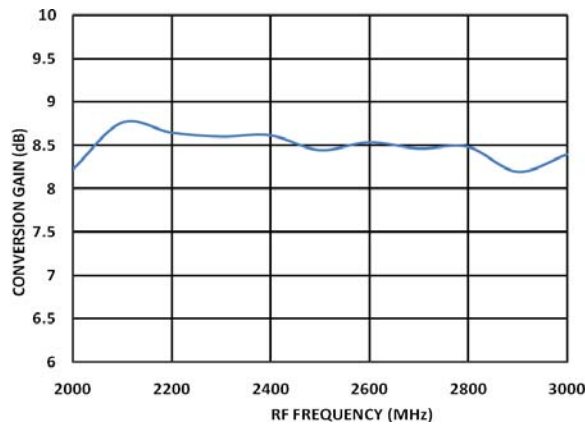


Figure 4. Power Conversion Gain vs. RF Frequency

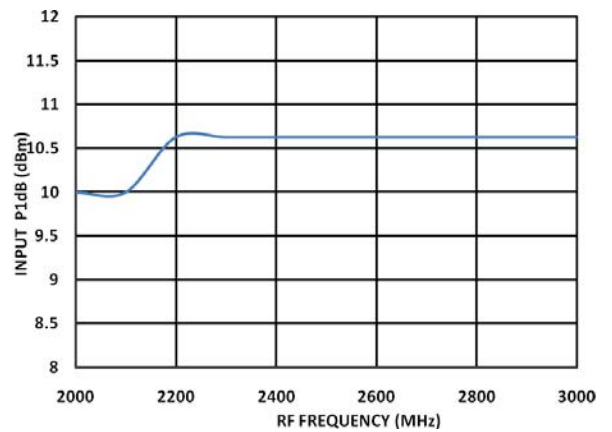


Figure 7. Input P1dB vs. RF Frequency

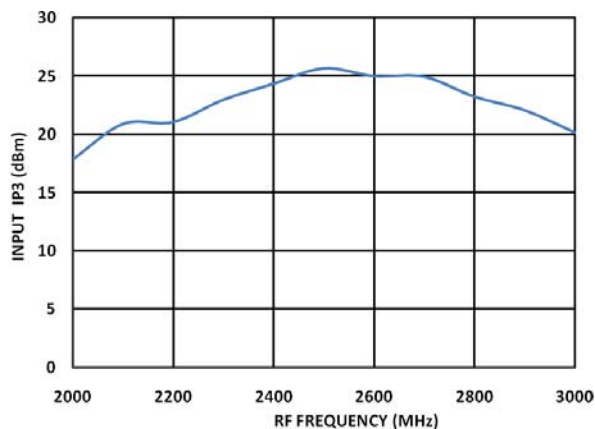


Figure 5. Input IP3 vs. RF Frequency

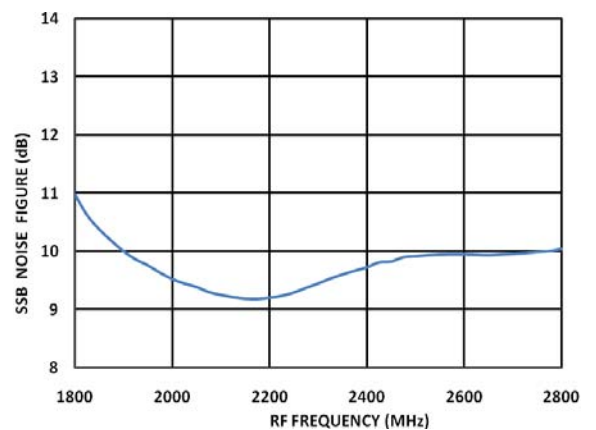


Figure 8. SSB Noise Figure vs. RF Frequency

CIRCUIT DESCRIPTION

The ADL5353 consists of two primary components: the radio frequency (RF) subsystem and the local oscillator (LO) subsystem. The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

The RF subsystem consists of an integrated, low loss RF balun, passive MOSFET mixer, sum termination network, and IF amplifier.

The LO subsystem consists of an SPDT-terminated FET switch and a three-stage limiting LO amplifier. The purpose of the LO subsystem is to provide a large, fixed amplitude, balanced signal to drive the mixer independent of the level of the LO input.

A block diagram of the device is shown in Figure 9.

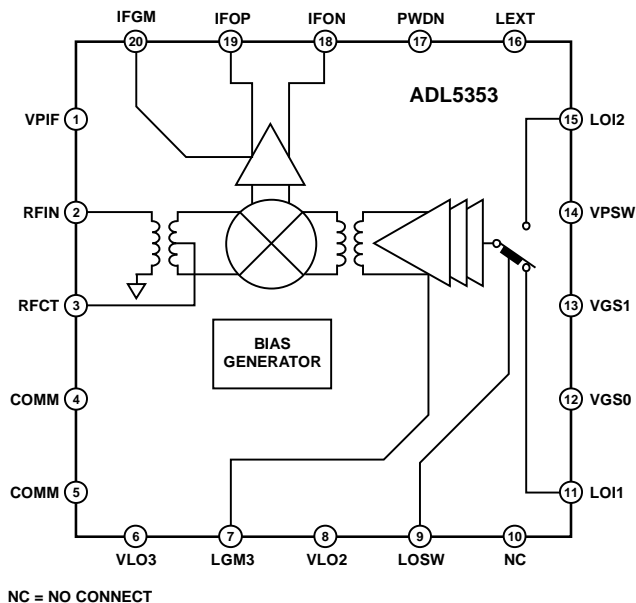


Figure 9. Simplified Schematic

RF SUBSYSTEM

The single-ended, 50 Ω RF input is internally transformed to a balanced signal using a low loss (<1 dB) unbalanced-to-balanced (balun) transformer. This transformer is made possible by an extremely low loss metal stack, which provides both excellent balance and dc isolation for the RF port. Although the port can be dc connected, it is recommended that a blocking capacitor be used to avoid running excessive dc current through the part. The RF balun can easily support an RF input frequency range of 2300 MHz to 2900 MHz.

The resulting balanced RF signal is applied to a passive mixer that commutates the RF input with the output of the LO subsystem. The passive mixer is essentially a balanced, low loss switch that adds minimum noise to the frequency translation. The only noise contribution from the mixer is due to the resistive loss of the switches, which is in the order of a few ohms.

As the mixer is inherently broadband and bidirectional, it is necessary to properly terminate all the idler ($M \times N$ product) frequencies generated by the mixing process. Terminating the mixer avoids the generation of unwanted intermodulation products and reduces the level of unwanted signals at the input of the IF amplifier, where high peak signal levels can compromise the compression and intermodulation performance of the system. This termination is accomplished by the addition of a sum network between the IF amplifier and the mixer and also in the feedback elements in the IF amplifier.

The IF amplifier is a balanced feedback design that simultaneously provides the desired gain, noise figure, and input impedance that is required to achieve the overall performance. The balanced open-collector output of the IF amplifier, with impedance modified by the feedback within the amplifier, permits the output to be connected directly to a high impedance filter, differential amplifier, or an analog-to-digital input while providing optimum second-order intermodulation suppression. The differential output impedance of the IF amplifier is approximately 200 Ω . If operation in a 50 Ω system is desired, the output can be transformed to 50 Ω by using a 4:1 transformer.

The intermodulation performance of the design is generally limited by the IF amplifier. The IP3 performance can be optimized by adjusting the IF current with an external resistor. Additionally, dc current can be saved by increasing either or both resistors. It is permissible to reduce the dc supply voltage to as low as 3.3 V, further reducing the dissipated power of the part. (Note that no performance enhancement is obtained by reducing the value of these resistors and excessive dc power dissipation may result.)

LO SUBSYSTEM

The ADL5353 has two LO inputs permitting multiple synthesizers to be rapidly switched with extremely short switching times (<40 ns) for frequency agile applications. The two inputs are applied to a high isolation SPDT switch that provides a constant input impedance, regardless of whether the port is selected, to avoid pulling the LO sources. This multiple section switch also ensures high isolation to the off input, minimizing any leakage from the unwanted LO input that may result in undesired IF responses.

The single-ended LO input is converted to a fixed amplitude differential signal using a multistage, limiting LO amplifier. This results in consistent performance over a range of LO input power. Optimum performance is achieved from -6 dBm to $+10$ dBm, but the circuit continues to function at considerably lower levels of LO input power.

The performance of this amplifier is critical in achieving a high intercept passive mixer without degrading the noise floor of the system. This is a critical requirement in an interferer rich environment, such as cellular infrastructure, where blocking interferers can limit mixer performance. The bandwidth of the intermodulation performance is somewhat influenced by the current in the LO amplifier chain. For dc current sensitive applications, it is permissible to reduce the current in the LO amplifier by raising the value of the external bias control resistor. For dc current critical applications, the LO chain

can operate with a supply voltage as low as 3.3 V, resulting in substantial dc power savings.

In addition, when operating with supply voltages below 3.6 V, the ADL5353 has a power-down mode that permits the dc current to drop to <200 μ A.

All of the logic inputs are designed to work with any logic family that provides a Logic 0 input level of less than 0.4 V and a Logic 1 input level that exceeds 1.4 V. All logic inputs are high impedance up to Logic 1 levels of 3.3 V. At levels exceeding 3.3 V, protection circuitry permits operation up to 5.5 V, although a small bias current is drawn.

All pins, including the RF pins, are ESD protected and have been tested up to a level of 1500 V HBM and 500 V CDM.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

The ADL5353 mixer is designed to downconvert radio frequencies (RF) primarily between 2300 MHz and 2900 MHz to lower intermediate frequencies (IF) between 30 MHz and 450 MHz. Figure 10 depicts the basic connections of the mixer. It is recommended to ac-couple RF and LO input ports to prevent non-zero dc voltages from damaging the RF balun or LO input circuit. The RFIN capacitor value of 3 pF is recommended to provide the optimized RF input return loss for the desired frequency band.

IF PORT

The mixer differential IF interface requires pull-up choke inductors to bias the open-collector outputs and to set the output match. The shunting impedance of the choke inductors used to couple dc current into the IF amplifier should be selected to provide the desired output return loss.

The real part of the output impedance is approximately 200 Ω , which matches many commonly used SAW filters without the need for a transformer. This results in a voltage conversion gain that is approximately 6 dB higher than the power conversion gain, as shown in Table 3. When a 50 Ω output

impedance is needed, use a 4:1 impedance transformer, as shown in Figure 10.

BIAS RESISTOR SELECTION

Two external resistors, $R_{BIAS\ IF}$ and $R_{BIAS\ LO}$, are used to adjust the bias current of the integrated amplifiers at the IF and LO terminals. It is necessary to have a sufficient amount of current to bias both the internal IF and LO amplifiers to optimize dc current vs. optimum IIP3 performance.

MIXER VGS CONTROL DAC

The ADL5353 features two logic control pins, VGS0 (Pin 12) and VGS1 (Pin 13), that allow programmability for internal gate-to-source voltages for optimizing mixer performance over desired frequency bands. The evaluation board defaults both VGS0 and VGS1 to ground.

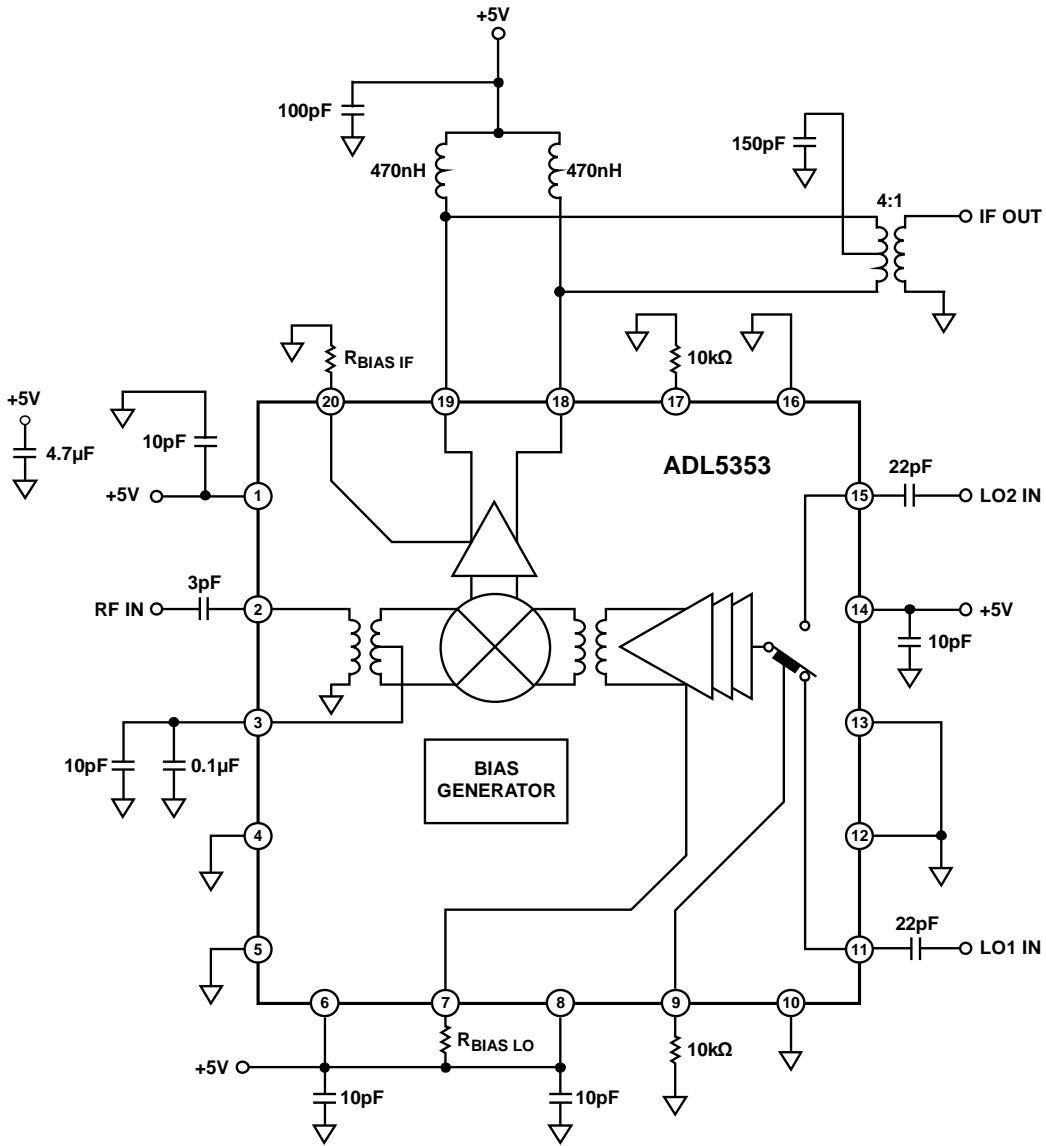


Figure 10. Typical Application Circuit

ADL5353-005

EVALUATION BOARD

An evaluation board is available for the family of double balanced mixers. The standard evaluation board schematic is shown in Figure 11. The evaluation board is fabricated using Rogers® RO3003 material. Table 6 describes the various configuration options of the evaluation board. Evaluation board layout is shown in Figure 12 to Figure 15.

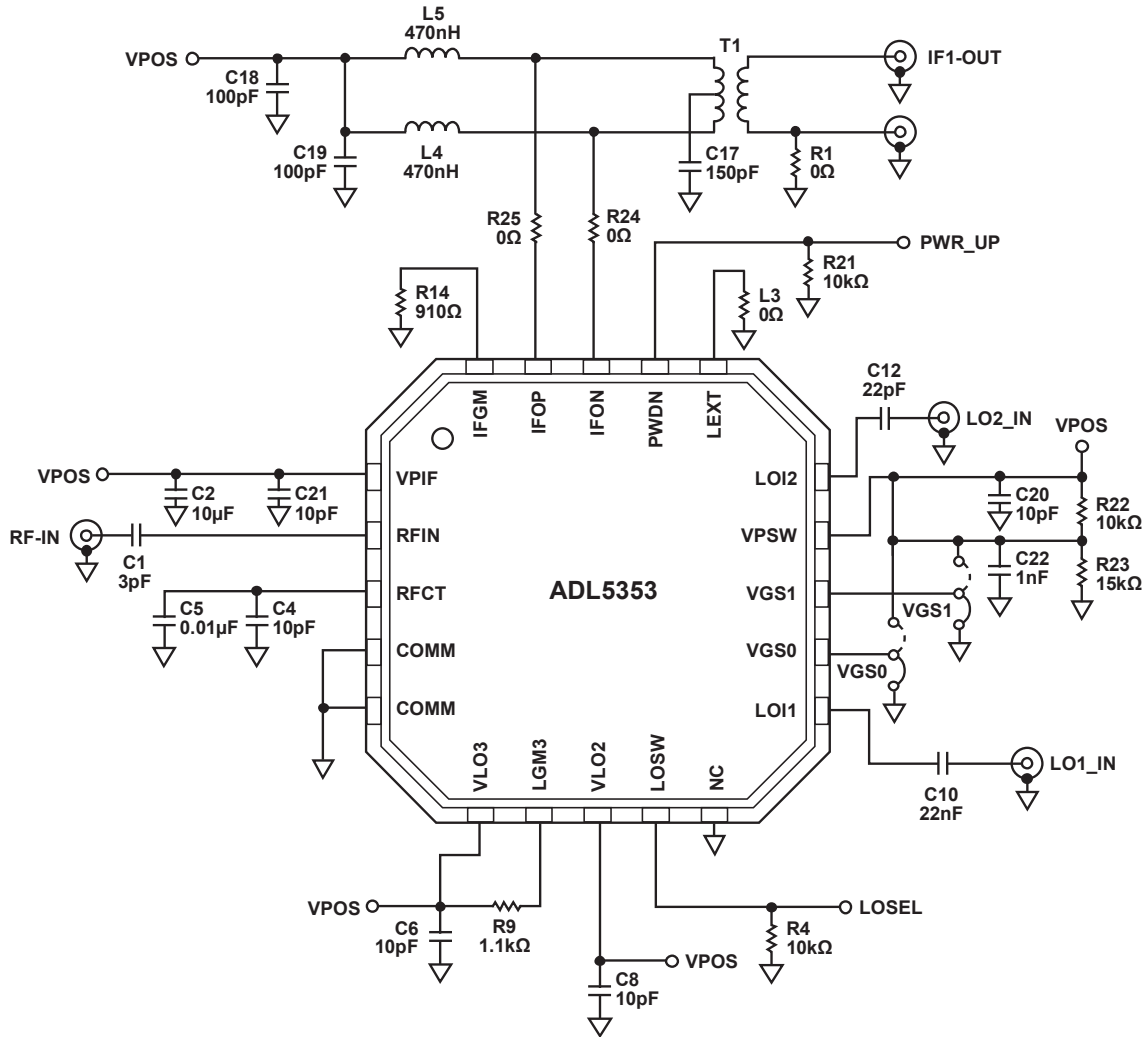


Figure 11. Evaluation Board Schematic

ADL5353-042

Table 6. Evaluation Board Configuration

Components	Description	Default Conditions
C2, C6, C8, C18, C19, C20, C21	Power Supply Decoupling. Nominal supply decoupling consists of a 10 μ F capacitor to ground in parallel with a 10 pF capacitor to ground positioned as close to the device as possible.	C2 = 10 μ F (size 0603), C6, C8, C20, C21 = 10 pF (size 0402), C18, C19 = 100 pF (size 0402)
C1, C4, C5	RF Input Interface. The input channels are ac-coupled through C1. C4 and C5 provide bypassing for the center taps of the RF input baluns.	C1 = 3 pF (size 0402), C4 = 10 pF (size 0402), C5 = 0.01 μ F (size 0402)
T1, C17, L4, L5, R1, R24, R25	IF Output Interface. The open-collector IF output interfaces are biased through pull-up choke inductors L4 and L5. T1 is a 4:1 impedance transformer used to provide a single-ended IF output interface, with C17 providing center-tap bypassing. Remove R1 for balanced output operation.	T1 = TC4-1W+ (Mini-Circuits), C17 = 150 pF (size 0402), L4, L5 = 470 nH (size 1008), R1, R24, R25 = 0 Ω (size 0402)
C10, C12, R4	LO Interface. C10 and C12 provide ac coupling for the LO1_IN and LO2_IN local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R4 provides a pull-down to ensure that LO1_IN is enabled when the LOSEL test point is logic low. LO2_IN is enabled when LOSEL is pulled to logic high.	C10, C12 = 22 pF (size 0402), R4 = 10 k Ω (size 0402)
R21	PWDN Interface. R21 pulls the PWDN logic low and enables the device. The PWR_UP test point allows the PWDN interface to be exercised using the external logic generator. Grounding the PWDN pin for nominal operation is allowed. Using the PWDN pin when supply voltages exceed 3.3 V is not allowed.	R21 = 10 k Ω (size 0402)
C22, L3, R9, R14, R22, R23, VGS0, VGS1	Bias Control. R22 and R23 form a voltage divider to provide 3 V for logic control, bypassed to ground through C22. VGS0 and VGS1 jumpers provide programmability at the VGS0 and VGS1 pins. It is recommended to pull these two pins to ground for nominal operation. R9 sets the bias point for the internal LO buffers. R14 sets the bias point for the internal IF amplifier.	C22 = 1 nF (size 0402), L3 = 0 Ω (size 0603), R9 = 1.1 k Ω (size 0402), R14 = 910 Ω (size 0402), R22 = 10 k Ω (size 0402), R23 = 15 k Ω (size 0402), VGS0 = VGS1 = 3-pin shunt

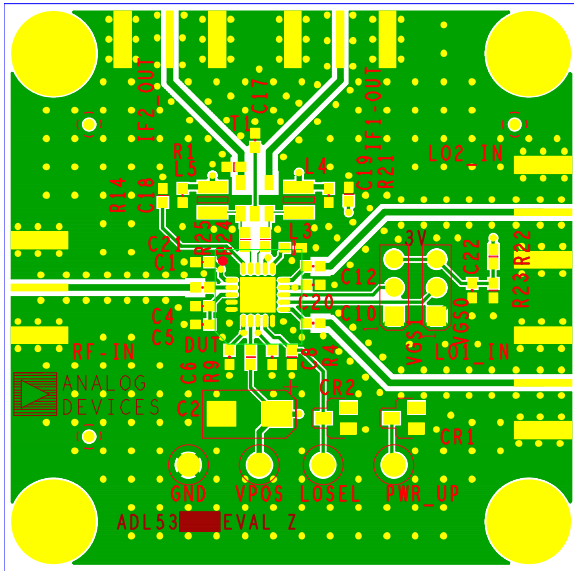


Figure 12. Evaluation Board Top Layer

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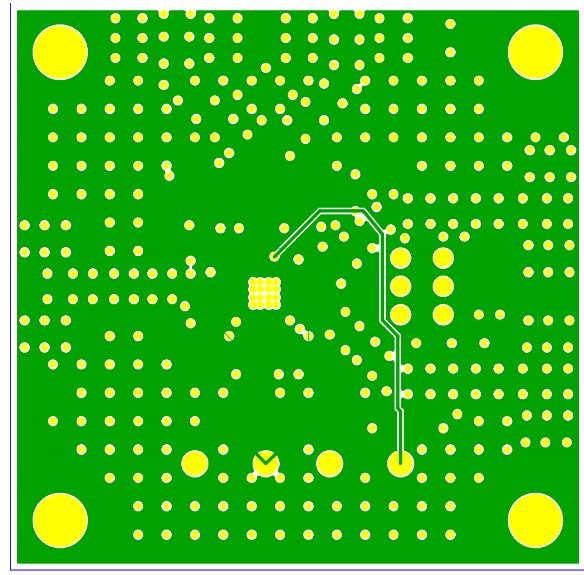


Figure 14. Evaluation Board Power Plane, Internal Layer 2

08080-057

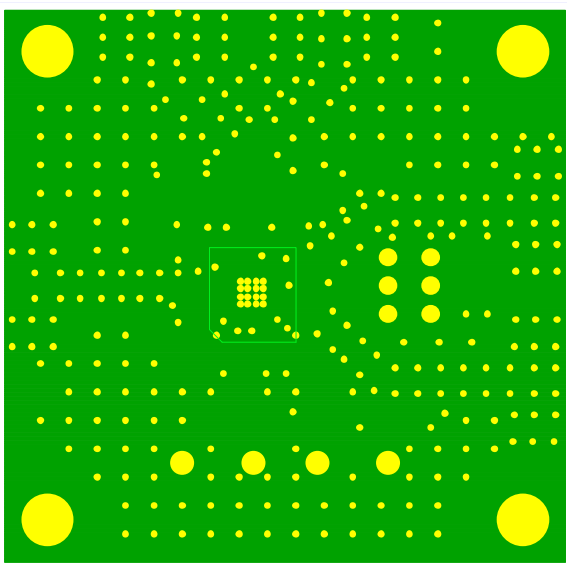


Figure 13. Evaluation Board Ground Plane, Internal Layer 1

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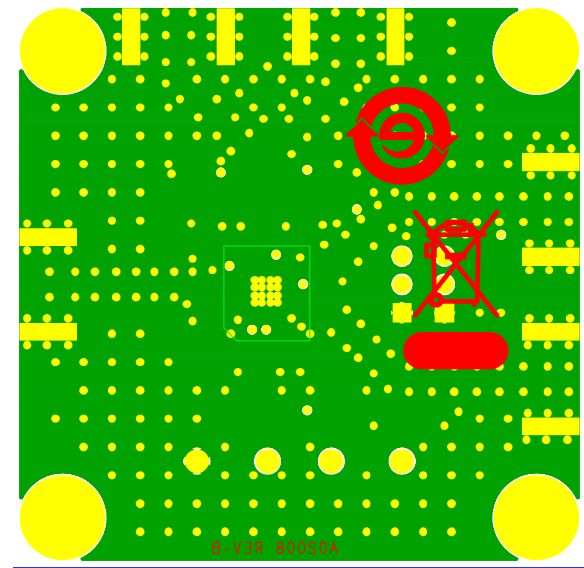
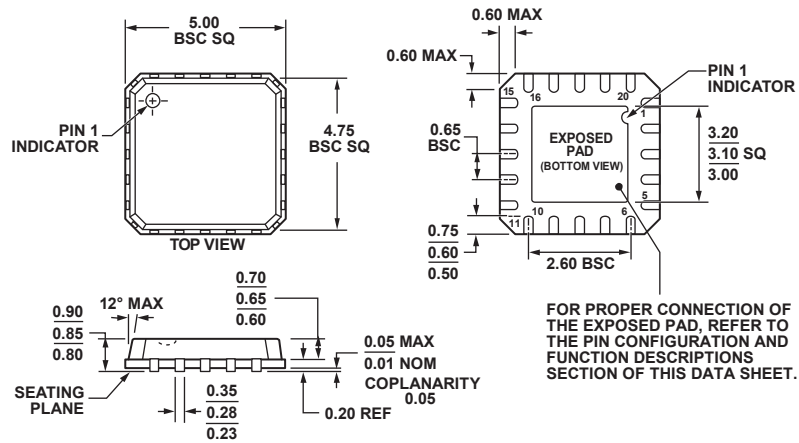


Figure 15. Evaluation Board Bottom Layer

08080-058

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHC

Figure 16. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad (CP-20-5)
Dimensions shown in millimeters

042205-B

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5353XCPZ-R7 ¹	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-5	1,500, 7" Tape and Reel
ADL5353XCPZ-WP ¹	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-20-5	36, Waffle Pack
ADL5353-EVALZ ¹		Evaluation Board		1

¹ Z = RoHS Compliant Part.

NOTES